REMARKS

Claims 12-22 are pending in the application. Claims 12 and 22 are the only independent claims.

Applicants note with thanks the withdrawal of the prior rejection of Claims 1-22 based on 35 USC 102(e) as being anticipated by Nam.

Section 103 rejection

Claims 12-22 were rejected under 35 USC 103(a) as being unpatentable over US Patent 6,211,018 B1 (Nam et al.) in view of Silicon Processing for the VLSI Era, Optical Photoresist Material Types, Pages 418-420, hereinafter "VLSI".

In view of the following discussion, each of the rejections is traversed and reconsideration is respectfully requested.

Independent Claim 12 recites that a *lateral thickness of said source region is independent of the measurement of the distance between the first and second apertures.*

Nam is directed to a method for fabricating high density trench gate type power devices, in which "1 or 2 masking processes are skipped unlike the conventional processes in which the well mask and the source mask are separately used" (abst.). In Nam's method, the insulating layer and the spacer insulating layer are used as etch masks to form a trench on the semiconductor substrate *and to define a source region* (col. 2, lines 47-49; col. 3, lines 2-5). As further described at col. 6, lines 45-50 of Nam, "as shown in FIG. 5E, the side wall spacers 76 and 77 are removed...[t]hen P or As is ion-implanted...and then, a heat treatment is carried out, thereby forming a source 81". Therefore, Nam does not teach or suggest a method of forming a trench MOSFET in accordance with Applicant's Claim 12, that specifically recites that "the lateral thickness of the source region is independent of the measurement of distance between the first and second apertures". VLSI also fails to provide such teaching or suggestion.

For at least the foregoing reason, it is respectfully submitted that independent Claim 12 is patentable over Nam and VLSI and reconsideration is requested.

Independent Claim 22 is directed to a method of forming a trench MOSFET including the steps recited in original Claim 12, but further recites, after the step of forming a trench in the epitaxial layer by etching the semiconductor wafer through the second aperture, ***removing the first masking material layer and the second masking material layer prior to performing the steps recited thereafter***.

Applicants respectfully note, in fact, that this limitation of independent Claim 22 is completely ignored in the Final Office Action - and is not addressed in any way as to any alleged teachings in either Nam or VLSI.

Nam and VLSI provide no teaching or suggestion of a method in accordance with Applicant's independent Claim 22 in which a step of "removing the first and second masking material layers" is performed before *forming an insulating layer lining at least a portion of the trench, forming a conductive region within the trench adjacent the insulating layer and forming a source region of said first conductivity type within an upper portion of the body region and adjacent the trench.*

Rather, as noted at col. 6, lines 38-46, "as shown in FIG. 5D, a gate oxide layer 78 is grown...on the inside walls of the trench...a phosphorus-doped polysilicon film is deposited....[t]hen, as shown in FIG. 5E, the side wall spacers 76 and 77 are removed..." (see also, col. 8, lines 24-28, steps (i) and (k)).

The teachings of Nam and VLSI, taken in combination, therefore fail to teach or suggest a method in accordance with each of independent Claims 12 and 22. For at least the foregoing reasons, Applicants respectfully submit that each of independent Claims 12 and 22 is patentable over the combined teachings Nam and VLSI and reconsideration is requested.

Dependent Claims 13-21 are believed to be clearly patentable for all of the reasons indicated above with respect to Claim 12, from which they depend, and even further distinguish over Nam and VLSI by reciting additional limitations. Should the Examiner be of the view that an interview would expedite consideration of the application, request is made that the Examiner

telephone the Applicants' attorney at (908) 518-7700 in order that any outstanding issues be resolved.

Respectfully submitted,

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